

## Claims

What is claimed is:

1        1. A method for implementing a redundancy enhanced differential  
2 signal interface comprising the steps of:  
3            detecting an error;  
4            responsive to said detected error, reducing an interface operating  
5 speed;  
6            alternately testing of true and complement sides of a differential  
7 signaling I/O pair; and  
8            responsive to detecting a failure of a true side or a complement side,  
9 setting the detected failed true side or complement side to a reference  
10 voltage and maintaining said reduced interface operating speed.

1        2. A method for implementing a redundancy enhanced differential  
2 signal interface as recited in claim 1 wherein the step of detecting said error  
3 includes the step of utilizing Error Correction Code (ECC) for error detecting.

1        3. A method for implementing a redundancy enhanced differential  
2 signal interface as recited in claim 1 wherein the step of reducing said  
3 interface operating speed includes the step of setting an interface operating  
4 speed to about one half of normal operating speed.

1        4. A method for implementing a redundancy enhanced differential  
2 signal interface as recited in claim 1 wherein the step of alternately testing  
3 true and complement sides of a differential signaling I/O pair includes the  
4 steps of providing a pair of multiplexers coupled to a differential receiver,  
5 each multiplexer receiving a respective true or complement signal first input  
6 and a voltage reference second input; and each multiplexer providing a  
7 respective true or complement output signal to said differential receiver.

1        5. A method for implementing a redundancy enhanced differential  
2 signal interface as recited in claim 4 includes the steps of enabling a  
3 multiplexer control for one of said pair of multiplexers; reading data; and  
4 checking for the error; and enabling a multiplexer control for the other one of  
5 said pair of multiplexers; reading data; and checking for the error.

1       6. A method for implementing a redundancy enhanced differential  
2 signal interface as recited in claim 1 further includes the steps responsive to  
3 detecting a failure of both said true side and said complement side, returning  
4 to normal operating speed and posting said failure.

1       7. A method for implementing a redundancy enhanced differential  
2 signal interface as recited in claim 1 further includes the steps responsive to  
3 detecting no failure of either a true side or a complement side, posting said  
4 detected no failure, and continuing operation at said reduced interface  
5 operating speed.

1       8. Apparatus for implementing a redundancy enhanced  
2 differential signal interface comprising:  
3           a differential signaling I/O pair;  
4           a differential receiver interface coupled to said differential signaling  
5 I/O pair; said differential receiver interface including a pair of multiplexers  
6 coupled to a differential receiver, each multiplexer having a first input  
7 receiving a respective true or complement signal and a second input  
8 connected to a voltage reference and a multiplexer control input; and each  
9 multiplexer providing a respective true or complement output signal to said  
10 differential receiver;  
11          error detecting means coupled to said differential receiver for  
12 detecting an error;  
13          test and failure control logic coupled to said error detecting means  
14 and said differential receiver interface; said test and failure control logic  
15 being responsive to a detected error, for reducing an interface operating  
16 speed; and alternately enabling said multiplexer control input of said pair of  
17 multiplexers for testing of true and complement sides of said differential  
18 signaling I/O pair; and responsive to detecting a failure of a true side or a  
19 complement side, for setting the detected failed true side or complement  
20 side to a reference voltage for continued operation.

1       9. Apparatus for implementing a redundancy enhanced  
2 differential signal interface as recited in claim 8 wherein said test and failure  
3 control logic maintains said reduced interface operating speed for continued  
4 operation after setting the detected failed true side or complement side to a  
5 reference voltage.

1           10. Apparatus for implementing a redundancy enhanced  
2 differential signal interface as recited in claim 8 wherein said test and failure  
3 control logic is responsive to detecting a failure of both said true side and  
4 said complement side, for returning to normal operating speed and for  
5 posting said detected failure of both said true side and said complement  
6 side.

1           11. Apparatus for implementing a redundancy enhanced  
2 differential signal interface as recited in claim 8 wherein said test and failure  
3 control logic is responsive to detecting no failure of either said true side and  
4 said complement side, for posting said no failure, and for maintaining said  
5 reduced interface operating speed for continued operation.

1           12. Apparatus for implementing a redundancy enhanced  
2 differential signal interface as recited in claim 8 wherein said reduced  
3 interface operating speed is about one half of normal operating speed.

1           13. Apparatus for implementing a redundancy enhanced  
2 differential signal interface as recited in claim 8 wherein said voltage  
3 reference is a middle level voltage between a high and low level of said  
4 differential signals.

1           14. Apparatus for implementing a redundancy enhanced  
2 differential signal interface as recited in claim 8 wherein said test and failure  
3 control logic tests true and complement sides of said differential signaling I/O  
4 pair includes by enabling said multiplexer control for one of said pair of  
5 multiplexers; reading data; and checking for the error; and enabling said  
6 multiplexer control for the other one of said pair of multiplexers; reading  
7 data; and checking for the error.